Distortion in Off-State Arsenide MESFET Switches

Robert H. Caverly

Abstract—**This paper presents the results of an investigation into the origin and level of distortion generated by the off-state gallium arsenide MESFET when used as a microwave semiconductor control element. The results show that the drain-gate and gate-source capacitance nonlinearities generate distortion in the device in its off-state. These nonlinearities, which reflect the capacitance-voltage characteristic of the capacitances, can be reduced in as-fabricated devices by increasing the gate reverse bias voltage. The level of distortion monotonically increases with frequency throughout the usable range of the MESFET when used in a series reflective switch. In an SPDT switch application, where both on and off-state devices are used, the distortion level is relatively constant at frequencies in the vicinity of the gate bias cut-off frequency. The nonlinear off-state model is compared with both a SPICE-based analysis, and with experimental data on a GaAs MESFET SPDT switch. The main conclusions to be drawn from the study are that the dominate distortion generated by a GaAs MESFET used in a switch application occurs in the on-state, and that off-state distortion can be only slightly improved in as-fabricated devices.**

I. Introduction

GALLIUM ARSENIDE (GaAs) metal-semiconductor field effect transistors (MESFET) offer significant advantages over other conventional semiconductor switching elements in many microwave and radio frequency (RF) switch and control applications. These advantages include low bias power consumption in both switch states, an inherent bias isolation of the MESFET, and easy incorporation into monolithic circuits. Like other semiconductor elements, the GaAs MESFET has electrical parameters that are nonlinear functions of the circuit currents and voltages, resulting in the generation of signals harmonically related to the excitation. The interest in distortion generated by GaAs MESFET control devices is timely since these devices are finding increased use communication systems. In applications such as cellular telephone systems, for example, multiple signals are simultaneously received and the generation of in-band intermodulation signals can seriously affect receiver sensitivity and the quality of both the transmitted and received signal.

In the design of circuits using GaAs MESFETs, a key design specification is the level of distortion introduced into the system. There have been several studies of the nonlinearities in MESFET switches [1], [2], but these have concentrated on the resistive nonlinearities of the MESFET in its on-state. The GaAs MESFET can, however, introduce distortion into a circuit while in its off-state as well due to the nonlinear dependence of the device capacitance on the microwave or RF signal amplitude. This paper presents the results of an investigation into the levels of distortion introduced by the off-state MESFET. An equivalent circuit for modeling the distortion in GaAs MESFETs in the off-state is presented and device and circuit factors that govern the distortion introduced by the device are discussed. The model is used in determining the distortion introduced by an off-state MESFET in a series reflective switch application. The results of the theoretical model are verified using SPICE, showing that the distortion level of the MESFET monotonically increases with frequency throughout the usable range of the MESFET. There is a change of slope, however, in the vicinity of the gate bias circuit cut-off frequency. In an SPDT switch application, where both on and off-state devices are used, the distortion level is relatively constant at frequencies in the vicinity of the gate bias circuit cut-off frequency. A comparison based on the distortion characteristics of a series connected GaAs MESFET switch in both switch states is discussed, indicating that the on-state distortion is at a much higher level than off-state distortion. Finally, the off-state model is combined with the on-state model of MESFET distortion [2] in comparing these models with experimental measurements on a GaAs SPDT switch.

Manuscript received November 11, 1991; revised November 30, 1992. This work was supported by Burlington Semiconductor Operations, M/A-COM, Inc., Burlington, MA.

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IEEE Log Number 9210205.

II. Theoretical Discussion

For a GaAs MESFET in its off-state, the gate of the transistor is dc biased well beyond pinch off so that the active layer is fully depleted. The resulting channel depletion region is modeled with capacitances between both gate and drain, and gate and source. These capacitances are in the RF path, and connected between these two capacitances is the external gate bias resistor R_G. This gate bias resistor is added to improve the bias isolation and allows the gate to float at the average channel potential at low frequencies [1], [3]. The primary capacitances in the RF path are the drain-gate and source-gate capacitances, C_{DG} and G_{GS}, respectively. Both the active layer depletion capacitances (C_{dg}, C_{gs}) as well as the layout sensitive extrinsic capacitances (C_{so}, C_{do}) make up both C_{DG} and C_{GS} (Fig. 1).

Takada *et al* [4] have developed expressions for the active layer depletion capacitance in terms of the drain-gate and gate-source voltages (V_{DG} and V_{GS}, respectively), and these relationships are repeated here

$$C_{DG}(t) = \varepsilon W \tan^{-1}\left[V_p/\{V_{bi} - V_p + V_{DG}(t)\}\right] + C_{do} \quad (1)$$

and

$$C_{GS}(t) = \varepsilon W \tan^{-1}\left[V_p/\{V_{bi} - V_p - V_{GS}(t)\}\right] + C_{so} \quad (2)$$

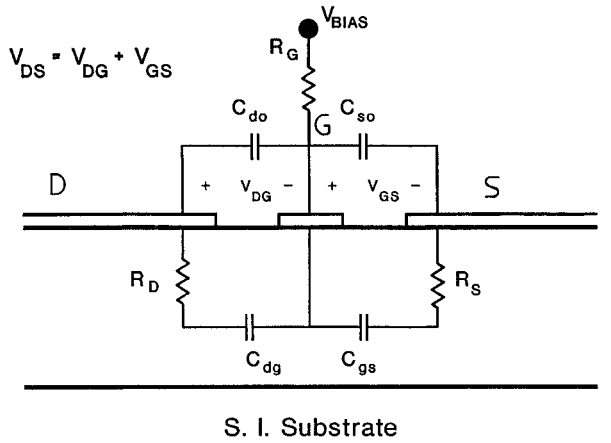


Fig. 1. A planar GaAs MESFET control structure, illustrating the origin of the device off-state capacitances, gate bias resistance and layout sensitive resistances and capacitances.

where ε is the permittivity of gallium arsenide, W is the gate width, V_p is the pinch-off potential and V_{bi} is the metal gate semiconductor junction potential. Under typical operating conditions, both V_{DG} and V_{GS} contain a dc term which sets the quiescent capacitance value, and an ac component that causes capacitance variations about this quiescent point capacitance. The larger the gate bias voltage, the lower both the quiescent capacitance and capacitance variations exhibited by the MESFET. However, the maximum dc gate bias level is limited by the gate breakdown voltage, which also affects the power handling capability of the circuit [1], [3]. The magnitude of the capacitance variation is dependent on the circuit topology and the ac voltage distribution in the circuit.

The combination of the time variation of the ac signal across the capacitance and the magnitude of the capacitance itself both contribute to the total distortion current in the off-state MESFET

$$i_{DG}(t) = d[C_{DG}(t)V_{DG}(t)]/dt \tag{3}$$

and

$$i_{GS}(t) = d[C_{GS}(t)V_{GS}(t)]/dt\,. \tag{4}$$

The solution of (3) and (4) for the distortion currents may be cast in the form of a power series. The derivation of closed form expressions for (3) and (4) is briefly outlined in Appendix A. The result shows that the level of the distortion currents is directly related to the variation of the capacitance with ac voltage, and is quantified by the expansion coefficients c_{gsn} and c_{gdn}. The primary factors controlling off-state GaAs MESFET distortion can be seen to be the gate bias voltage V_{io}, the pinch off voltage V_p and the gate width W. Of these factors, only the gate bias voltage V_{io} can be varied in as-fabricated devices.

In the design of practical microwave systems, one of the interests of microwave circuit designers is the minimization, or at least control, of second-order harmonic and third-order intermodulation distortion. By limiting the discussion of the MESFET nonlinearities to second- and third-order distortion, only the first two expansion coefficients of the power series need to be considered

TABLE I

Gate Width	1000 micron
Gate Length	1 micron
Channel Depth	0.2 micron
V_p	3 volts
V_{bi}	0.8 volts
R_G	2000 Ω
Z_o	50 Ω
N_{chan}	10^{17} cm^{-3}

$$c_{gs1} = \frac{\varepsilon W}{2}\,\frac{1}{V_{bi}-V_{io}}\sqrt{\frac{V_p}{V_{bi}-V_p-V_{io}}}\,\frac{F}{V} \tag{5}$$

$$c_{gs2} = \frac{1}{2}c_{gs1}\left[\frac{1}{2V_p}\,\frac{V_p}{V_{bi}-V_p-V_{io}} + \frac{1}{V_{bi}-V_{io}}\right]\frac{F}{V^2}\,. \tag{6}$$

From (5) and (6), c_{gs1} and c_{gs2} represent the amplitude and phase of the current nonlinearities introduced by the C_{GS} in response to the ac voltage. A similar result can be applied to C_{DG}. Equations (5) and (6) show that the harmonic currents generated in as-fabricated MESFETs can be reduced only by increasing the reverse bias on the gate electrode (V_{io}). The absolute limits of this reverse bias voltage are the pinch-off voltage at the lower limit, and the gate breakdown voltage at the upper limit [1]. An appropriate bias point for both distortion and power handling would lie approximately midway between these two voltages [1], [3].

The frequency dependence of the distortion generated by the MESFET is influenced by the gate bias circuit cut-off frequency f_G, where f_G is approximately $1/2\pi R_G(C_{DG}+C_{GS})$. The exact frequency dependence of the device nonlinearities is a strong function of the circuit topology and the distribution of ac voltage across the gate-drain and gate-source electrodes. In series connected MESFETs, the majority of the input voltage is dropped across C_{DG} at low frequencies, making this capacitance the major contributor to the low-frequency nonlinearities. The resulting distortion current, however, is isolated from the load because of the high reactance of C_{GS} at low frequencies, resulting in low load distortion levels. As the frequency of operation increases toward f_G and beyond, V_{DG} and V_{GS} become comparable in magnitude and produce similar distortion currents, resulting in an increase in distortion throughout the circuit. A similar result holds for shunt connected MESFETs as well.

The level of distortion introduced to the load by any nonlinear circuit element can be represented using the concept of distortion intercept point. Even though these intercept points are extrapolated power levels since compression of the fundamentals occurs at high power levels, they do provide a single figure of merit for distortion level comparison [5]. The dependence of distortion on frequency and MESFET parameters may be illustrated by using the following parameters which are typical for small signal switching MESFETs (Table I).

Typical switching MESFETs have identical drain-gate and gate-source electrode spacing, making the layout sensitive capacitances identical. This spacing is typically in the range

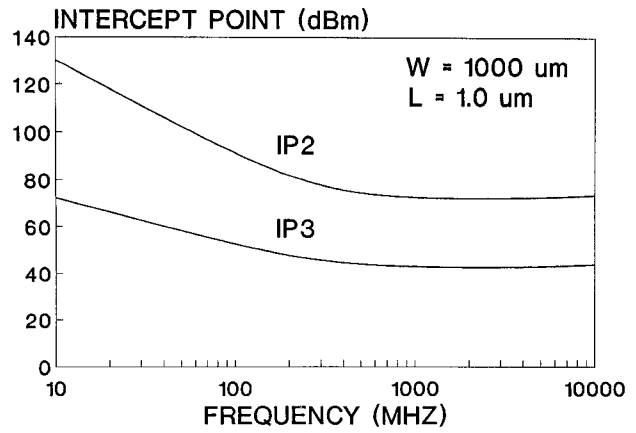


Fig. 2. Second and third order harmonic intercept point referenced to the source versus frequency for a 1000 micrometer gate width control MESFET biased at twice the pinch off voltage. Note that at frequencies above several hundred megahertz, the intercept points are relatively constant with frequency.

of one to two microns as a compromise between minimizing off-state interelectrode capacitance and on-state channel to electrode resistance. Fig. 2 illustrates calculations of off-state harmonic intercept point at a 50 Ω load for a series connected GaAs MESFET switch biased at twice the pinch off voltage. The intercept point decreases with increasing frequency, indicating increasing load distortion levels. The change in slope above approximately 100 MHz (which is in the vicinity of f_G for the device), shows the effects of nonlinearities produced by both G_{DG} and C_{GS}. The relatively constant intercept point at frequencies above f_G can be explained using (1) and (2) For example, on the positive swing of the source voltage, there is an instantaneous decrease in the value of C_{DG} and a corresponding instantaneous increase in C_{GS}. The resulting distortion currents partially cancel each other and track with frequency since V_{DG} and V_{GS} are comparable in magnitude above f_G. The lower intercept point at frequencies above f_G occurs because of the increased frequency, and hence increased distortion current magnitude [(3) and (4)].

The results of the theoretical model have been compared with SPICE simulations [6], [7]. The SPICE simulations use the Curtice model [6] for the MESFET gate-source and gate-drain capacitances. Fig. 3(a) and 3(b) shows results of calculations of isolation, and IP2 and IP3, for the series connected MESFET switch using both the theoretical model and SPICE. There is good agreement with all the parameters throughout the usable frequency range of this GaAs MESFET, indicating the validity of this theoretical model. The usable range of this device is defined as an isolation of greater than 20 dB, which is approximately 2.0 GHz for this device.

The gate width of the MESFET controls such switch parameters as on-state insertion loss, off-state isolation and device power handling. In the off-state, increasing the gate width increases the off-state capacitance and switching speed, lowers the load isolation, and increases the distortion currents flowing though the load. On the other hand, an increase in gate width improves the power handling, and lowers the distortion of the GaAs MESFET in the on-state [1]–[3], [8]. Fig. 4 illustrates the role of gate width on distortion intercept point, assuming an

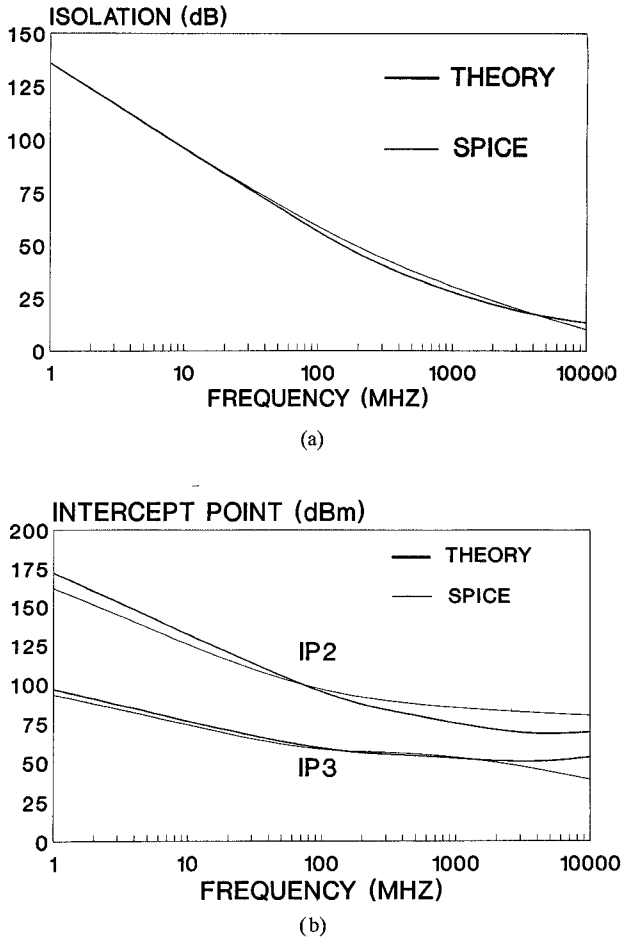


Fig. 3. Off-state isolation (a), and second and third order distortion intercept point (b) results using the theoretical model and the Curtice model [6] in SPICE. Note the relatively good agreement between the two models, with the SPICE results slightly underestimating the distortion intercept point.

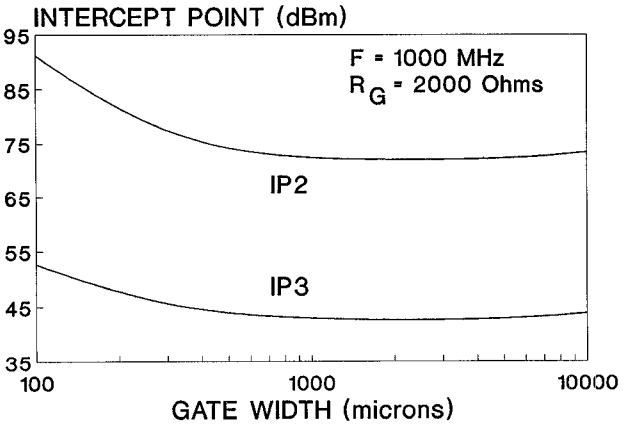


Fig. 4. Second and third order harmonic intercept point referenced to the source versus MESFET gate width for operation at the gate bias circuit cut-off frequency. Note that MESFETs with gate widths greater than approximately 1000 micrometers show nearly constant distortion with increasing gate width.

operating frequency at the gate bias circuit cut-off frequency. The results show that intercept point decreases with increased gate width due to lower load isolation and increased capacitive nonlinearity [see (1) and (2)]. There is little to be gained in terms of off-state distortion for devices with gate widths

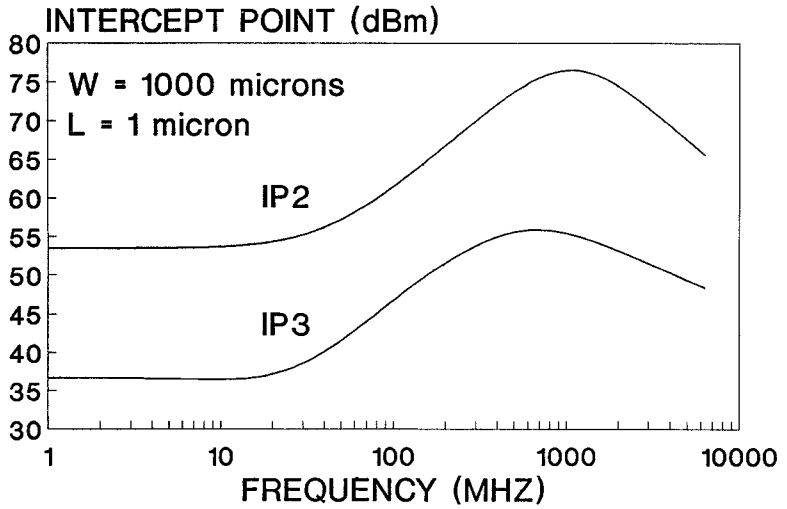


Fig. 5. Plot of the second and third order harmonic intercept point versus frequency for a series connected GaAs MESFET in the on-state. The data in Table I were used in the calculations. The on-state MESFET distortion is based on the model presented in [2].

above approximately 1000 microns. As stated earlier, however, an increase in gate width will improve power handling and decrease the on-state distortion. Similar trends in intercept point exist for other frequencies of operation.

III. Discussion

A. Comparison of MESFET Distortion in Both Switch States

The on-state distortion in a GaAs MESFET in a switch configuration is governed by the nonlinearities in the channel resistance, with a frequency dependence caused by a shift in the MESFET operating point occurring near the gate bias cut-off frequencies f_G. This operating point change shifts the MESFET into a more linear operating region at frequencies above f_G, causing lower signal distortion [2]. Using this on-state GaAs MESFET distortion model and the parameters listed in Table I, the on-state distortion in a SPDT GaAs MEFET switch was calculated. Fig. 5 presents these calculations in terms of the frequency dependence of the on-state second- and third-order distortion intercept points referenced to the load. Fig. 5 shows that the load distortion levels are lower for the off-state MESFET at all frequencies; however, the difference decreases with increasing frequency. In an RF application using passive MESFET switches, the dominate distortion occurs in the on-state. In addition, there is little that can be done external to the switch to improve this distortion. The intercept point transition frequency can be shifted to lower frequencies, however, by increasing R_G with the addition of an external gate bias resistor. This approach can also improve low-frequency power handling, but at the expense of slower switching speed [9].

B. Experimental Results—GaAs MESFET SPDT Switch

Distortion measurements were performed using a commercial surface mount SPDT GaAs MESFET (M/A-COM/ANZAC SW-239) switch (Fig. 6) to test the validity of the model. In the SPDT switch configuration used in these experiments, the series element is in the off-state whereas the element in shunt with the input port is in the on-state. The distortion contribution of both elements must be included when comparing the overall distortion appearing at the load. This is modeled by using the superposition principle with the on-state resistive and off-state capacitive nonlinear currents at the load. The nonlinear response of the on-state MESFET used as a switch and control element has been published elsewhere [2] and is included in comparing the data with the model. In all measurements, the input power level was kept below 13 dBm and all unused ports were terminated in 50 Ω loads to ensure that the series MESFET channel region remained fully depleted during the entire RF swing. Distortion measurement procedures discussed by Caverly and Hiller [10] were used. Fig. 6 shows a comparison between both theoretical and experimental data of the off-state of the SPDT switch. The model shows reasonably good agreement with the experimental results, with some overestimation of the distortion level at the load. From the results indicated in Fig. 3(b), SPICE using the Curtice Model [6] also tends to overestimate the off-state distortion as well. The nearly constant intercept point in the 10 MHZ to 1000 MHZ range is due to the contribution of both the on-state and off-state MESFETs in the SPDT switch. Third-order distortion measurements are not presented because the small power level of the distortion components were too low to be measured.

IV. Conclusion

The objective of this investigation was to give a better understanding of the level of distortion generated by the GaAs MESFET in a control application by the capacitive nonlinearities in the off-state. The fundamental conclusion reached is that the level of distortion generated at a given frequency depends on the gate width and bias level of the MESFET and the frequency of operation with respect to the gate bias circuit cut-off frequency. Increasing the MESFET gate width will improve characteristics such as power handling capability and on-state distortion, but will generally cause a deterioration

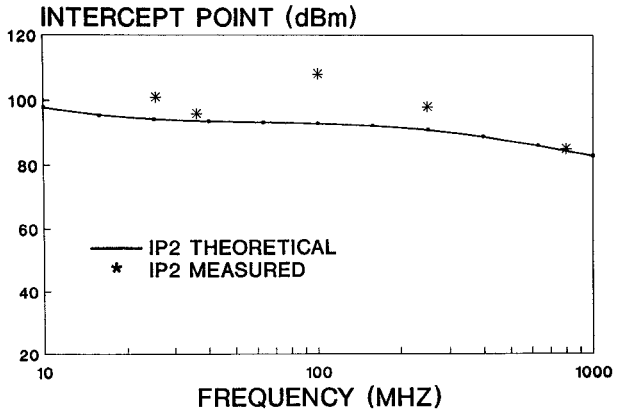


Fig. 6. Plot of a comparison between theoretical calculations and experimental measurements of second order harmonic intercept point versus frequency for a SPDT MESFET switch in its off (isolated) state.

in the off-state isolation and distortion, and an increase in switching speed due to increased device capacitance.

The model outlined in this paper now allows prediction of distortion generated by the GaAs MESFET as a control device in both of its passive operational states. At low frequencies (typically below f_G), a series connected GaAs MESFET control device in the off-state will generate distortion several orders of magnitude less than in the on-state. At frequencies in the UHF range and beyond, both switch states have more comparable distortion, although the off-state distortion is still less. It is the on-state distortion that is the dominate distortion in GaAs MESFET switches and should be considered in the design of passive MESFET control circuits.

Appendix A

Analyzing the distortion generated by the off-state MESFET requires the determination of the nonlinear equivalent circuit distortion currents generated by the circuit capacitances and expressed in (3) and (4). The capacitances C_{DG} and G_{GS} are functions of time through their dependence on the circuit voltage drops $V_{DG}(t)$ and $V_{GS}(t)$, respectively. Focusing on C_{GS}, the voltage dependent capacitance may be written as a power series in powers of $V_{GS}(t)$

$$C_{GS}(t) = \sum_{n=0}^{\infty} c_{gsn} V_{GS}^{n}(t) \tag{A1}$$

where the c_{gsn} are the power series coefficients and are derived from derivatives of the expression for $C_{GS}(t)$ in (2). A similar result holds for $C_{DG}(t)$. If $V_{GS}(t)$ is assumed to have an $e^{j\omega t}$ variation, then the nonlinear gate-source current $i_{GS}(t)$ may be written as

$$i_{GS}(t) = \sum_{n=0}^{\infty} j\omega(n+1) c_{gsn} V_{GS}^{n+1}(t). \tag{A2}$$

In a similar fashion, the nonlinear drain-gate current may be written as

$$i_{DG}(t) = \sum_{n=0}^{\infty} j\omega(n+1) c_{dgn} V_{DG}^{n+1}(t). \tag{A3}$$

In most applications, the voltages $V_{GD}(t)$ and $V_{GS}(t)$ consist of signals with different amplitudes, and must be described by a collection of sinusoids

$$V_{GS}(t)^{V_{GS}(t)=Z\cdots} \sum_{k=1}^{K} V_k \cos \omega_k t = \frac{1}{2} \sum_{k=-K}^{K} V_k e^{j\omega_k t} \tag{A5}$$

where $V_{-k} = V_K^*$ and $\omega_{-k} = -\omega_k$. Substituting (A5) into (A1) and (A2) gives the total varying current through the gate capacitor C_{GS} in the presence of multiple signals:

$$i_{GS}(t) = \sum_{n=0}^{\infty} \sum_{k=-K}^{K} j\omega_k(n+1) \cdot c_{gsn} 2^{-(n+1)} V_k e^{j\omega_k t} \left[\sum_{k=-K}^{K} V_k e^{j\omega_k t} \right]^n \tag{A6}$$

with a similar result for $i_{DG}(t)$. The minimization of these currents for n greater than zero (the nonlinear terms) requires minimization of the c_{gsn}, which, by inspecting (5) and (6), can only be done by increasing the gate reverse bias well beyond pinch off. These expressions describe the equivalent distortion circuit distortion generators for the GaAs MESFET in the off-state in terms of the frequency of operation, MESFET construction (through the term c_{gsn}) and the voltage $V_{GS}(t)$.

Acknowledgment

The author wishes to thank Gerald Hiller of Burlington Semiconductor Operations, M/A-COM Inc., Burlington, MA, and Peter A. Rizzi of the Department of Electrical and Computer Engineering of the University of Massachusetts—Dartmouth for critically reading the manuscript and providing valuable suggestions. The author also wishes to thank Gerald Hiller for our many interesting, and sometimes entertaining, discussions on the applications of semiconductor control devices.

References

[1] R. Gutmann, and D. Fryklund, "Characterization of linear and nonlinear properties of GaAs MESFETs for broad-band control applications," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-35, no. 4, pp. 516–520, May 1987.

[2] R. Caverly, "Distortion in broad-band gallium arsenide MESFET control and switch circuits," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-39, no. 4, pp. 713–717, Apr. 1991.

[3] N. Jain, and R. Gutmann, "Modeling and design of gallium arsenide MESFET control devices for broad-band applications," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-38, no. 2, pp. 109–117, Feb. 1990.

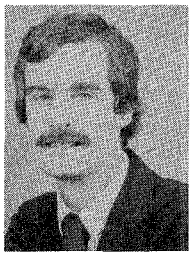
[4] T. Takada, K. Yokoyama, M. Ida, and T. Sudo, "An MESFET variable capacitance model for gallium arsenide integrated circuit simulation," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-30, no. 5, pp. 719–723, May 1982.

[5] G. Heiter, "Characterization of nonlinearities in microwave devices and systems," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-21, pp. 797–804, Dec. 1973.

[6] W. R. Curtice, "An MESFET model for use in the design of GaAs integrated circuits," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-28, pp. 448–456, May 1980.

[7] H. Statz, P. Newman, I. Smith, R. Pucel, and H. Haus, "GaAs FET device and circuit simulation in SPICE," *IEEE Trans. Electron Devices*, vol. ED-34, no. 2, pp. 160–169, Feb. 1987.

[8] A. Gopinath and J. Rankin, "GaAs FET RF switches," *IEEE Trans. Electron Devices,* vol. ED-32 no. 7, pp. 1272–1278, July 1985.
[9] R. Gutmann and N. Jain, "Comments on GaAs MESFET baseband-to-microwave passive switches," *IEEE Trans. Microwave Theory Tech.,* vol. MTT-37, no. 7, pp. 1154–1155, July 1989.
[10] R. Caverly and G. Hiller, "Distortion in p-i-n diode control circuits," *IEEE Trans. Microwave Theory Tech.,* vol. MTT-35, no. 5, pp. 492–501, May 1987.



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Dr. Caverly is the author of more than twenty technical papers in the areas of microwave device modeling and integrated circuit design. He is a past recipient of the Dow Outstanding Young Faculty Award from the American Society of Engineering Education, and is a member and faculty advisor of the local student chapter of Eta Kappa Nu, the electrical Engineering Honor Society.